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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1 53(b))

Attorney Docket No. 0756-2077

First Inventor or Application Identifier: Shunpei YAMAZAKI

Title: INSULATING FILM FORMED USING AN ORGANIC SILANE AND METHOD OF PRODUCING SEMICONDUCTOR DEVICE

Express Mail Label No.

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form (e.g., PTO/SB/17)
   (Submit an original, and a duplicate for fee processing)
2. [X] Specification *Total Pages* [18]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 USC 113) *Total Sheets* [3]
4. [X] Oath or Declaration *Total Pages* [3]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 17 completed)
   [Note Box 5 below]
   i [ ] DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [X] Incorporation By Reference *(useable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission
   (if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement [ ] Power of Attorney
   (when there is an assignee)
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement [ ] Copies of IDS
    (IDS)/PTO-1449 Citations
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503)
    (Should be specifically itemized)
14. [ ] *Small Entity Statement(s) (PTO/SB/09-12) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s)
    (if foreign priority is claimed)
16. [ ] Other:

*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. **If a CONTINUING APPLICATION**, *check appropriate box, and supply the requisite information below and in a preliminary amendment.*
    Divisional of prior application No. 09/190,828 filed November 12, 1998; which itself is a Divisional of application Serial No. 08/734,127 filed October 21, 1996; which is a Continuation of Serial No. 08/445,574 filed May 31, 1995; which is a Divisional of Serial No. 08/198,054 filed February 18, 1994.
    Prior application information: Examiner: S. Loke Group/Art Unit: 2811

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Signature Date: December 20, 1999

Docket: 0756-2077

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re DIVISIONAL Application of)
Shunpei YAMAZAKI et al.)
Based On Serial No. 09/190,828) Art Unit: 2811
Which Was Filed: November 12, 1998) Examiner: S. Loke
For: INSULATING FILM FORMED)
USING AN ORGANIC SILANE)
AND METHOD OF PRODUCING)
SEMICONDUCTOR DEVICE) Date: December 20, 1999

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please preliminarily amend the subject application as follows:

IN THE SPECIFICATION:

Before the first sentence of the specification, insert --This application is a Divisional of Application Serial No. 09/190,828 filed November 12, 1998; which itself is a Divisional of application Serial No. 08/734,127 filed October 21,

1996; which is a Continuation of Serial No. 08/445,574 filed May 31, 1995; which is a Divisional of Serial No. 08/198,054 filed February 18, 1994.--

REMARKS

This application has been amended to include the continuing application data thereof.

Examination on the merits is requested.

Respectfully submitted,

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Registration No. 38,285

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TITLE OF THE INVENTION

INSULATING FILM AND METHOD OF PRODUCING SEMICONDUCTOR DEVICE

FIELD OF THE INVENTION

The present invention relates to a method for producing a gate-insulating film which is used in a thin film device such as a gate-insulated field effect transistor or the like, at a low temperature of 650°C or lower, and also to the insulating film produced by the method.

BACKGROUND OF THE INVENTION

Heretofore, in a thin film device such as a gate-insulated field effect thin-film-transistor (TFT) or the like, a silicon oxide film with good characteristics, which is obtained by forming a crystalline silicon followed by heating and oxidizing its surface at high temperatures falling within a range of from 900 to 1100°C, has been used as a gate-insulating film.

The oxide film formed by such thermal oxidation is essentially characterized in that its interfacial level density is extremely low and that it may be formed on the surface of a crystalline silicon at a uniform thickness. Accordingly, the former brings about good on/off characteristics and long-term reliability on bias/temperature; while the latter reduces the short circuit between a gate electrode and a semiconductor area (active layer) at the edges in an island semiconductor region to thereby improve the production yield of semiconductor devices.

To use such a thermal oxide film in producing semiconductor devices, however, a material which is resistant to high temperatures must be selected as the material for the substrate. In this respect, since inexpensive glass materials (for example, alkali-free glass such as Corning 7059, etc.) cannot be used, the production costs are disadvantageously high especially when

large-area substrates are used. Recently, a technical means for forming TFT on an alkali-free substrate is being developed, in which, however, a thermal oxide film cannot be used but a gate-insulating film shall be formed by sputtering or by physical or chemical vapor deposition (CVD) such as plasma CVD or reduced pressure CVD.

However, it was inevitable that the characteristics of the silicon oxide film formed by such means were inferior to those of the thermal oxide film. Namely, the interfacial level density of the former is generally large and, additionally, the former was always accompanied by the dangers of alkali ions such as sodium ions or the like invading the film being formed. In addition, since the step coverage of the silicon oxide film is not so good, the film frequently caused the short circuit between the gate electrode and the active layer at the edges of the island semiconductor region. For these reasons, it was extremely difficult to obtain semiconductor devices of the kind satisfying all the characteristics, the reliability and the production yield by the prior art technology.

SUMMARY OF THE INVENTION

The present invention has been made so as to solve at least one of these problems in the prior art technology. Accordingly, one object of the present invention is to provide a method for producing a silicon oxide film with good step coverage. Another object of the present invention is to provide a silicon oxide film which is resistant to unfavorable impurities such as alkali ions and others and also to provide a method for producing the film.

First, the present invention is characterized in that a film which has been obtained by plasma CVD using a mixed gas containing an organic silane having ethoxy groups, oxygen, and

hydrogen chloride or a chlorine-containing hydrocarbon, as the raw material gas, and consists essentially of silicon oxide is used as a gate-insulating film.

Secondly, the present invention is also characterized in that a film which has been obtained by plasma CVD using a mixed gas containing an organic silane having ethoxy groups, oxygen, and a fluorine-containing gas (e.g., NF_3, C_2F_6), as the raw material gas, and consists essentially of silicon oxide is used as a gate-insulating film.

Accordingly, the present invention provides an insulating film consisting essentially of silicon oxide, which has been formed on an island non-monocrystalline semiconductor region consisting essentially of silicon to closely cover the region and is characterized in that from 1 x 10^{17} to 5 x 10^{20} cm^{-3} of halogens are detected from the film by secondary mass spectrometry and that 5 x 10^{19} cm^{-3} or less carbons are detected therefrom.

The present invention also provides a first method of producing a semiconductor device comprising a first step for forming an island non-monocrystalline semiconductor region consisting essentially of silicon and a second step for forming a film consisting essentially of silicon oxide over the non-monocrystalline semiconductor region in a plasma atmosphere resulting from a mixed gas containing an organic silane having ethoxy groups, oxygen, and hydrogen chloride or a chlorine-containing hydrocarbon.

The present invention further provides a second method of producing a semiconductor device comprising a first step for forming an island non-monocrystalline semiconductor region consisting essentially of silicon, a second step for exposing the island semiconductor region to a plasma atmosphere containing oxygen, and hydrogen chloride or a chlorine-containing

hydrocarbon, and a third step for forming a film consisting essentially of silicon oxide over the non-monocrystalline semiconductor region in a plasma atmosphere resulting from a mixed gas containing an organic silane having ethoxy groups and oxygen.

BRIEF EXPLANATION OF THE DRAWINGS

Fig.1(A) is a conceptual cross-sectional view showing a positive column CVD apparatus used in an example of the present invention.

Fig.1(B) is a conceptual plan view showing the positive column CVD apparatus shown in Fig.1(A).

Figs. 2(A) to 2(E) shows a flow sheet showing the formation of TFT in the example.

Fig. 3 shows the characteristic curves of breakdown voltage of the insulating films obtained in the example.

Figs. 4(A) and 4(B) show the characteristic curves of V_{FB} of the insulating films obtained in the example.

DETAILED DESCRIPTION OF THE INVENTION

As the organic silane having ethoxy groups, preferred are substances to be represented by chemical formulae $Si(OC_2H_5)_4$ (tetraethoxysilane, hereinafter referred to as TEOS), $Si_2O(OC_2H_5)_6$, $Si_3O_2(OC_2H_5)_8$, $Si_4O_3(OC_2H_5)_{10}$ and $Si_5O_4(OC_2H_5)_{12}$. Since these organic silane materials move on the surface of the substrate for a long period of time to be decomposed on the surface to form a silicon oxide film thereon, they may well get into even hollows to give an excellent film with good step coverage.

As the chlorine-containing hydrocarbon, preferred are substances to be represented by chemical formulae C_2HCl_3 (trichloroethylene), $C_2H_3Cl_3$ (trichloroethane) and CH_2Cl_2

preferred to add to the atmosphere hydrogen chloride or a chlorine-containing material such as trichloroethylene, trichloroethane, dichloromethane or the like, in addition to oxygen, to further improve the effect.

On the other hand, after the formation of the insulating film consisting essentially of silicon oxide by the above-mentioned method, the film may further be heat-treated at temperatures falling within the range of from 200 to 650°C to thereby reduce the fluctuations of the flat band potential. The heat treatment is preferably conducted in an oxygen-free atmosphere such as argon, nitrogen or the like. The fluctuations of the flat band potential are noticeably reduced by the heat treatment at 450°C or higher and the reduction is saturated at 600°C or higher.

The second method of the present invention is characterized by comprising exposing an island non-monocrystalline semiconductor region consisting essentially of silicon to a plasma atmosphere containing oxygen, and hydrogen chloride or a chlorine-containing hydrocarbon, followed by forming a film consisting essentially of silicon oxide over the non-monocrystalline semiconductor region by plasma CVD using a raw material containing an organic silane having ethoxy groups and oxygen.

In the second method, hydrogen chloride or a chlorine-containing hydrocarbon is essentially accumulated in the chamber during the plasma treatment, which brings about the same effect as that to be brought about by the above-mentioned first method where hydrogen chloride or a chlorine-containing hydrocarbon is added, during the following step of forming the silicon oxide film. The same as that mentioned above shall apply to the second step with respect to the improvement in the reliability attainable by the plasma treatment. To obtain a better result

from the second method, it is also preferred that the chlorine concentration and the carbon concentration in the silicon oxide film thus formed by the second method are the same as those in the film formed by the above-mentioned the first method. It is also preferred in the second method that the film consisting essentially of silicon oxide thus formed is subjected to heat treatment at 200 to 650°C, preferably at 450 to 600°C, after the filming in order to obtain a further better result.

The plasma CVD apparatus to be employed in the present invention may be either an ordinary parallel plate-type apparatus (in which a pair of electrode plates are located in a chamber, facing to each other, and one or both of them has/have a sample substrate mounted thereon) or a positive column-type apparatus such as that used in the following example.

However, the latter is preferred to the former in view of the following two points. One is that the amount of the substrates to be treated at one time is determined by the area of the electrodes used in the former, while it is determined by the discharging volume in the latter. Accordingly, a larger amount of substrates may be processed at one time by the latter. The other is that the surface of the substrate treated by the former is much damaged by the plasma, while the latter is almost free from the damage by the plasma since it has almost no potential inclination. In addition, since the uniformity of the film to be formed using the latter is better than that using the former, the uniform film has no bad influences on the characteristics of TFT and the production yield thereof.

It is necessary that the chamber of the plasma CVD apparatus to be used for the filming in the present invention is sufficiently cleaned, prior to its use, so as to reduce the content of alkali elements, such as sodium, etc., in the chamber. To clean the chamber, chlorine, hydrogen chloride or the above-

mentioned chlorine-containing hydrocarbon may be introduced into the chamber along with oxygen, and thereafter the plasma may be generated therein. It is preferred that the chamber is heated at 150°C or higher, preferably 300°C or higher, so as to more effectively carry out the step.

EXAMPLE

This example demonstrates one embodiment of the present invention of forming a silicon oxide film, as the gate-insulating film, on an island non-monocrystalline silicon semiconductor film by positive column plasma CVD, essentially showing the electric characteristics of the silicon oxide film formed. The plasma CVD apparatus used herein is shown in Fig. 1. Fig. 1(A) is a vertical cross-sectional view of the apparatus, and Fig. 1(B) is a top plan view of the same. The positive column CVD is characterized in that the substrate to be coated is located in the positive column region for plasma discharging and is coated with films therein.

The RF power sources 102 and 103 give the power to generate plasma. Regarding the frequency from the sources, radio waves are typically employed, having a frequency of 13.56 MHz. The power fed from the two power sources is adjusted by the phase shifter 104 and the matching boxes 105 and 106 in such a way that the condition of the plasma to be formed is the best. The power derived from the RF power sources arrives at the pair of electrodes 107 and 108 that have been located in parallel to each other in the inside of the chamber 101 and have been protected by the electrode covers 112 and 113, thus causing discharging between these electrodes. Substrates to be treated are located between the electrodes 107 and 108. In order to improve the mass-producibility, the substrates 111 are cased in a container 109, where they are attached to the both surfaces of the sample

holders 110. The substrates are characterized in that they are parallel to each other between the electrodes. The substrates are heated by the infrared lamp 114 and kept at suitable temperatures. Though not shown, the apparatus is fitted with a gas exhauster and a gas-feeding means.

The filming conditions and the characteristics of the film formed are mentioned below. The temperature of the substrates was 300°C. Into the chamber, 300 SCCM of oxygen, 15 SCCM of TEOS and 2 SCCM of trichloroethylene (hereinafter referred to as TCE) were introduced into the chamber. The RF power was 75 W, and the whole pressure was 5 Pa. After the filming, the film formed was annealed in hydrogen atmosphere at 350°C for 35 minutes.

Fig. 3 shows the results of the dielectric breakdown test of the silicon oxide films of 1000 Å thick that had been formed on high-resistance silicon wafers using the present apparatus. Over the silicon oxide film, formed was a 1 mmø-aluminum electrode and the relation between the voltage and the current was plotted. Fig. 3(C) indicates the film that had been formed on the substrate without any particular treatment of the substrate prior to the filming, from which it is noted that the breakdown voltage of the film is low. The films of Fig. 3(A) were formed as follows: After the substrates were set in the chamber, they were heated at 300°C and exposed to the plasma atmosphere generated by introducing 400 SCCM of oxygen and from 0 to 5 SCCM of TCE. The total pressure of the atmosphere was 5 Pa, and the RF power was 150 W. The plasma exposure was carried out for 10 minutes. (During the step, no film was formed by the gaseous reaction.) After the plasma exposure, the silicon oxide films of Fig. 3(A) were formed, and they showed a high breakdown voltage.

The films of Fig. 3(B) were formed as follows in the same manner as in Fig. 3(A) except that the flow rate of TCE in the filming step was changed to 4 SCCM or more, for example 5 SCCM.

As shown, they had a low breakdown voltage. From these results, it has been found that the TCE concentration for the filming has the optimum value.

Fig. 4(A) shows the result of the bias/temperature test, as one example of the reliability tests, of the insulating films formed in this example, indicating the relation between the fluctuations (V_{FB}) of the flat band voltage (V_{FB}) and the pre-treatment, if any, of the substrates. In the bias/temperature test, a voltage of +17 V was imparted to the sample at 150°C for one hour and the C-V characteristic of the sample was measured at room temperature. Next, a voltage of -17 V was imparted to the same sample at 150°C for one hour and the C-V characteristic thereof was also measured at room temperature. The difference in V_{FB} between the two measurements was obtained to be V_{FB}.

In Fig. 4(A), the substrate of the sample (a) was not pre-treated. V_{FB} of the sample (a) was about 5 V and was relatively large. However, the problem was solved by pre-treating the substrate. The substrates of the samples (b) and (c) were pre-treated under the conditions mentioned below.

Sample	(b)	(c)
Temperature of Substrate	300°C	300°C
TCE/Oxygen	0/400	0.5/400
RF Power	150 W	150 W
Time for Treatment	10 min	10 min

From Fig. 4(A), it is understood that the reliability of the insulating film was improved much more by pre-treating the substrate using TCE.

The same improvement may also be attained by annealing the insulating film formed. The annealing of the film was carried out in argon of one atmospheric pressure at 300 to 570°C for one

hour. The relation between the annealing temperature and V_{FB} is shown in Fig. 4(B), from which it is noted that V_{FB} was significantly reduced when the film was annealed at temperatures not higher than 450°C, while it became gradually constant when the annealing temperature was being near to 600°C. From the result, it was clarified that the annealing of the insulating film formed is effective in improving the reliability of the film.

On the basis of the results obtained from the above-mentioned experiments, a TFT sample was produced. The flow sheet for producing it is shown in Fig. 2. First, the silicon oxide film 202 of 2000 Å thick was formed, as a subbing film, on the substrate (Corning 7059) 201, by positive column plasma CVD using TEOS, oxygen and TCE as raw materials. The apparatus used herein was same as that shown in Fig. 1. The main conditions for the filming were as follows:

Temperature of Substrate:		300°C
Whole Pressure:		5 Pa
Mixed Gas:		
TOES:	12 SCCM	
Oxygen:	300 SCCM	
TCE:	2 SCCM	
RF Power:		75 W

Next, an amorphous silicon film of 500 nm thick was deposited thereover by plasma CVD, and this was patterned to form the island silicon region 203. This was allowed to stand in nitrogen atmosphere at 400°C for 30 minutes to remove hydrogen therefrom. Next, this was annealed with a laser ray, as shown in Fig. 2(A), to crystallize the silicon region. As the laser, used was a KrF excimer laser (having a wavelength of 248 nm and a

pulse width of 20 nsec). The energy density was from 200 to 350 mM/cm^2. During the irradiation of the laser rays, the substrate was kept at 300 to 500°C, for example 450°C.

Afterwards, the silicon oxide film 204 of 1000 Å thick was formed to cover the island silicon region 203, as a gate-insulating film, by positive column plasma CVD using TEOS, oxygen and TCE as raw materials, as shown in Fig. 2(B). Prior to the filming, the substrate was pre-treated, using the same apparatus as in Example 1. The main conditions for the pre-treatment were as follows:

Temperature of Substrate:	300°C
Whole Pressure:	5 Pa
Mixed Gas:	
Oxygen:	400 SCCM
TCE:	0.5 SCCM
RF Power:	150 W
Time for Treatment:	10 minutes

After the pre-treatment, the film 204 was formed. The main condition for the filming were mentioned below. After the filming, the film formed was annealed in argon atmosphere at 550°C for one hour.

Temperature of Substrate:	300°C
Whole Pressure:	5 Pa
Mixed Gas:	
TEOS:	15 SCCM
Oxygen:	300 SCCM
TCE:	2 SCCM
RF Power:	75 W

Next, a 2% silicon-doped aluminum film of 6000 Å thick was deposited over the film and this was patterned to form the gate electrode 205. Then, impurity ions (phosphorus or boron) were introduced into the region 203 in a self-ordered manner by plasma doping, using the gate electrode 205 as the mask, to form the impurity regions 206 and 207, as shown in Fig. 2(C). The area into which the impurities had not been introduced became the channel-forming region 208. Since the doping was conducted through the gate-insulating film, it needed an accelerated voltage of 80 kV for phosphorus and 65 kV for boron. The dose amount was suitable from 1 x 10^{15} to 4 x 10^{15} cm^{-2}.

Next, the impurities were activated also by annealing with laser rays, as shown in Fig. 2(D). As the laser, used was the KrF excimer laser (having a wavelength of 248 nm and a pulse width of 20 nsec). The energy density was from 200 to 350 mJ/cm^2. During the irradiation of the laser rays, the substrate may be kept at 300 to 500°C. After the irradiation of the laser rays, this was annealed at 350°C in hydrogen atmosphere having a partial pressure of from 0.1 to 1 atmospheric pressure for 35 minutes.

Next, the silicon oxide film 209 of 5000 Å thick was deposited thereover as an interlayer insulating film. The silicon oxide film 209 was formed by positive column CVD, using TEOS, oxygen and TCE as raw materials. The apparatus used for the filming was the same as in Example 1. The main conditions for the filming were as follows:

Temperature of the Substrate:	300°C
Whole Pressure:	5 Pa
Mixed Gas:	
TEOS:	30 SCCM
Oxygen:	300 SCCM

RF Power: 100 W

Afterwards, the contact holes 210 and 122 were formed through the interlayer insulating film, and the electrodes 212 and 213 were formed as a source and a drain, respectively, of TFT, using aluminum. In place of aluminum, also usable are titanium and titanium nitride. In this manner mentioned above, TFT was completed. The production yield of TFT was extremely improved, since the step coverage of the gate-insulating film was improved and the reliability of the gate-insulating film was improved.

As mentioned above in detail, the silicon oxide film of the present invention has sufficient reliability as a gate-insulating film. In addition, it has become obvious that the present invention contributes to not only the improvement in the reliability of the film but also the improvement in the production yield. Moreover, the mass-producibility of the device of the present invention may be improved, using the positive column plasma CVD apparatus such as that employed in the example. Thus, the present invention is useful as an industrial invention.

While the invention has been described in detail and with reference to specific embodiments thereof, it will be apparent to one skilled in the art that various changes and modifications can be made therein without departing from the spirit and scope thereof.

WHAT IS CLAIMED IS:

1. A method of forming an insulating film comprising silicon oxide formed over a glass substrate,

wherein the insulating film includes halogen at a concentration of $5x10^{20}$ cm^{-3} or less and carbon at a concentration of $5x10^{19}$ cm^{-3} or less which are detected by second ion mass spectroscopy.

2. A method according to claim 1, wherein the halogen is fluorine or chlorine.

3. A method according to claim 1, wherein the insulating film includes carbon at a concentration of $1x10^{18}$ cm^{-3} or less which is detected by the second ion mass spectroscopy.

4. A method according to claim 1, wherein said insulating film is a gate insulating film.

5. A method according to claim 1 wherein the insulating film is an insulating film in a thin film transistor.

6. A method according to claim 1, wherein the insulating film covers an even surface over the glass substrate.

7. A method according to claim 1, wherein the insulating film includes halogen at a concentration of 1×10^{17} cm^{-3} or more.

8. A method of producing a semiconductor device, said method comprising the steps of:

forming a crystalline semiconductor island formed over a glass substrate; and

forming an insulating film including silicon oxide formed to cover the crystalline semiconductor island,

wherein the insulating film includes halogen at a concentration of $5x10^{20}$ cm^{-3} or less and carbon at a concentration of $5x10^{19}$ cm^{-3} or less.

9. A method according to claim 8, wherein the concentrations of halogen and carbon are detected by secondary ion mass spectroscopy.

10. A method according to claim 8, wherein the halogen is fluorine or chlorine.

11. A method according to claim 8, wherein the insulating film is formed by plasma chemical vapor deposition using an organic silane.

12. A method according to claim 8, wherein the insulating film includes halogen at a concentration of 1×10^{17} cm^{-3} or more.

13. A method of fabricating a thin film transistor, said method comprising the steps of:

forming a crystalline semiconductor island formed over a glass substrate;

forming a silicon oxide film formed to cover the crystalline semiconductor island; and

forming a conductive film including at least one of aluminum, titanium, and titanium nitride, said conductive film being formed on the silicon oxide film,

wherein the silicon oxide film includes halogen at a concentration of $5x10^{20}$ cm^{-3} or less and carbon at a concentration of $5x10^{19}$ cm^{-3} or less.

14. A method according to claim 13, wherein the halogen is fluorine or chlorine.

15. A method according to claim 13, wherein the silicon oxide film is formed by plasma chemical vapor deposition using an organic silane.

16. A method according to claim 13, wherein the silicon oxide film includes halogen at a concentration of 1×10^{17} cm^{-3} or more.

17. A method of fabricating a thin film transistor, said method comprising the steps of:

forming a crystalline semiconductor island formed over a glass substrate;

forming a gate insulating film including silicon oxide formed on the crystalline semiconductor island; and

forming a gate electrode formed on the insulating film,

wherein the gate insulating film includes halogen at a concentration of 5×10^{20} cm^{-3} or less and carbon at a concentration of 5×10^{19} cm^{-3} or less.

18. A method according to claim 17, wherein the halogen is fluorine or chlorine.

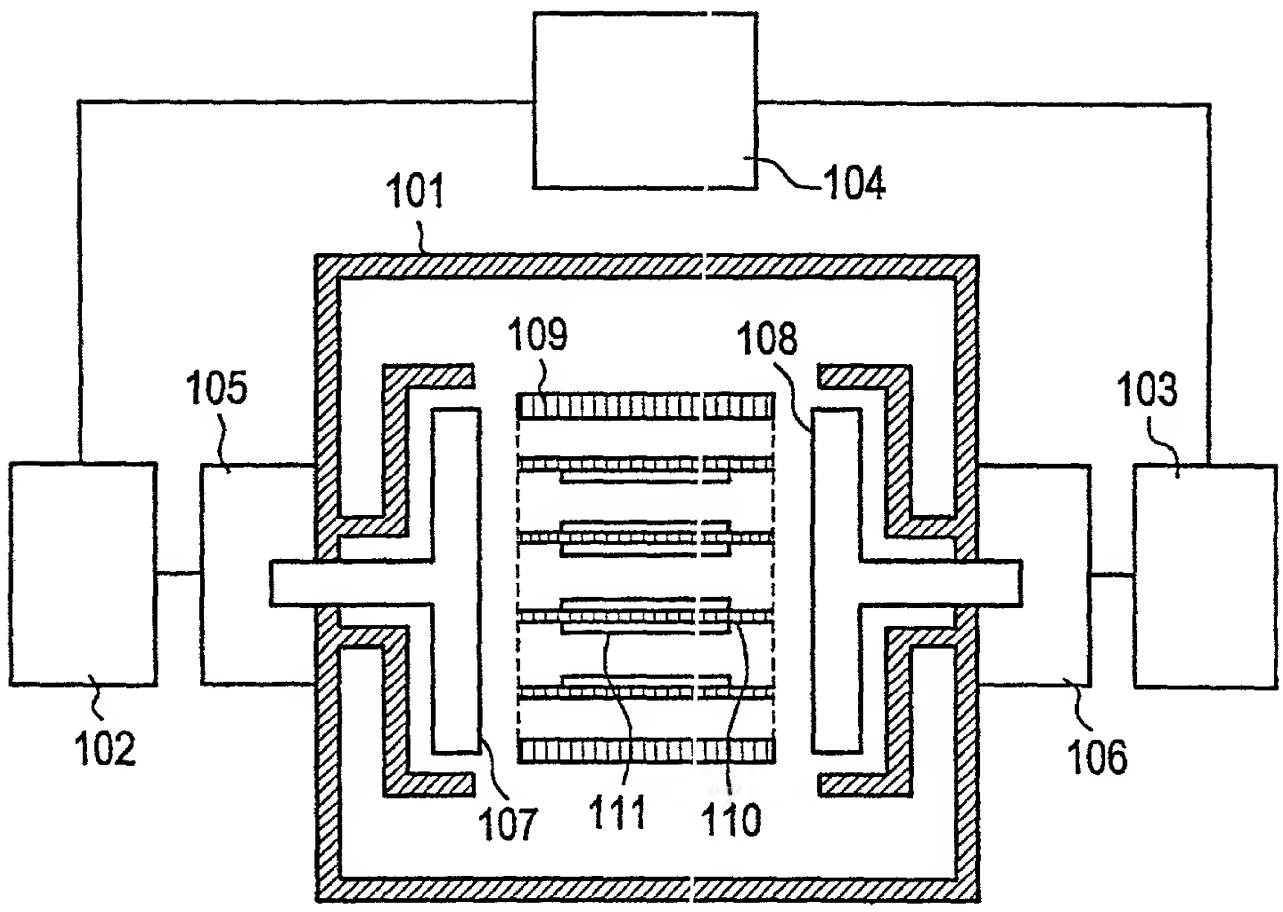
19. A method according to claim 17, wherein the gate insulating film is formed by plasma chemical vapor deposition using an organic silane.

20. A method according to claim 17, wherein the gate insulating film includes halogen at a concentration of 1×10^{17} cm^{-3} or more.

ABSTRACT OF THE DISCLOSURE

A silicon oxide film is formed to cover an island non-monocrystalline silicon region by plasma CVD using an organic silane having ethoxy groups (e.g., TEOS) and oxygen as raw materials, while hydrogen chloride or a chlorine-containing hydrocarbon (e.g., trichloroethylene) of a fluorine-containing gas is added to the plasma CVD atmosphere, preferably in an amount of from 0.01 to 1 mol% of the atmosphere so as to reduce the alkali elements from the silicon oxide film formed and to improve the reliability of the film. Prior to forming the silicon oxide film, the silicon region may be treated in a plasma atmosphere containing oxygen and hydrogen chloride or a chlorine-containing hydrocarbon. The silicon oxide film is obtained at low temperatures and this has high reliability usable as a gate-insulating film in a semiconductor device.

FIG.1A


104
101
109
108
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103
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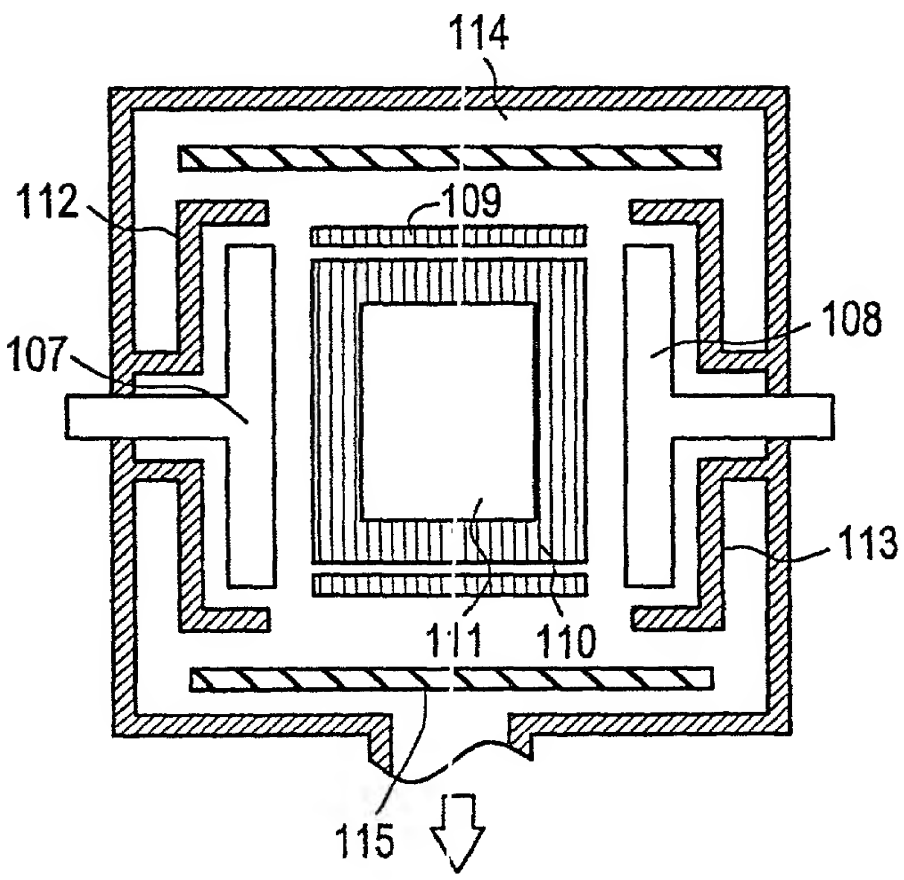
111
110

FIG.1B


114
112
109
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107
113
111
110
115

FIG.2A

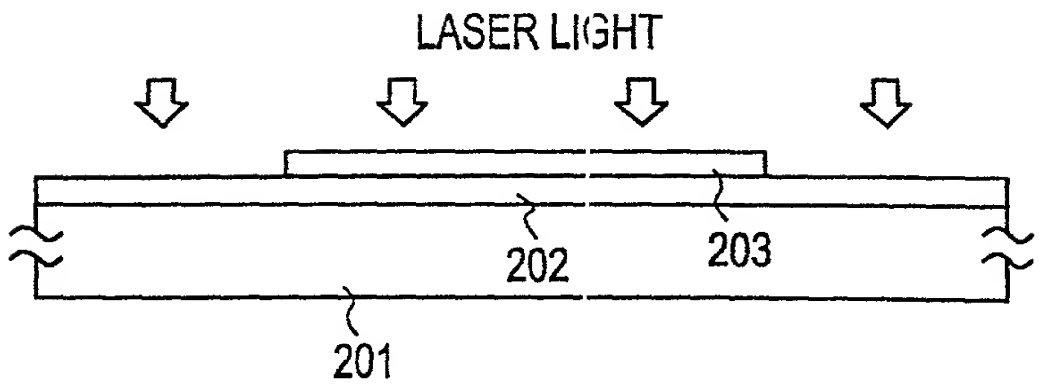


FIG.2B

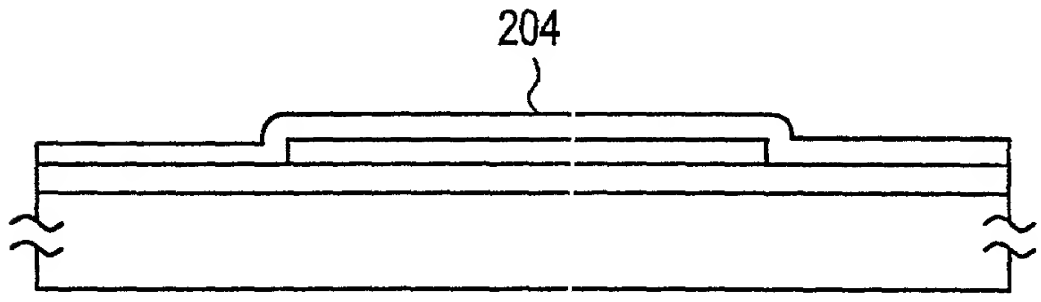


FIG.2C

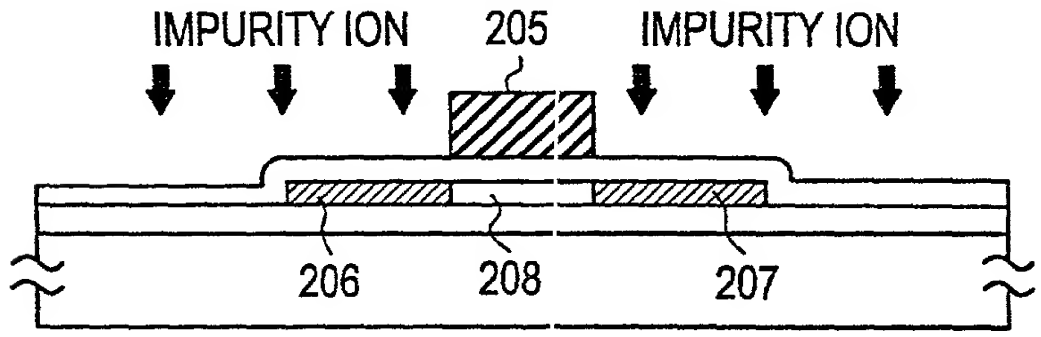


FIG.2D

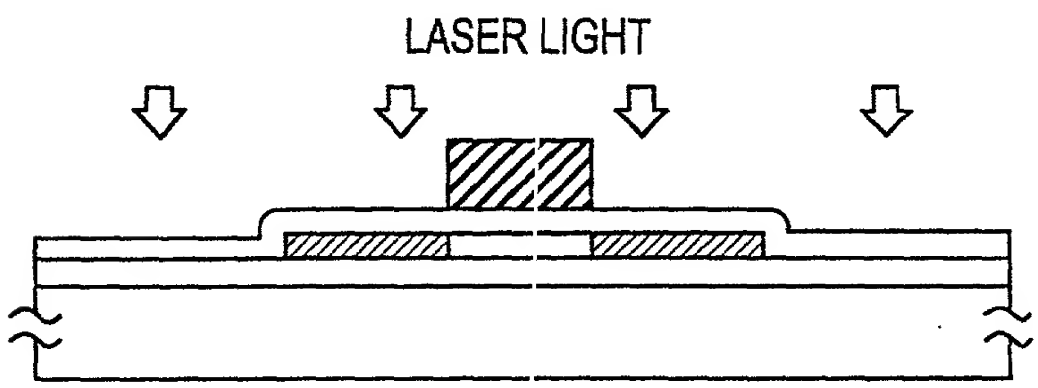


FIG.2E

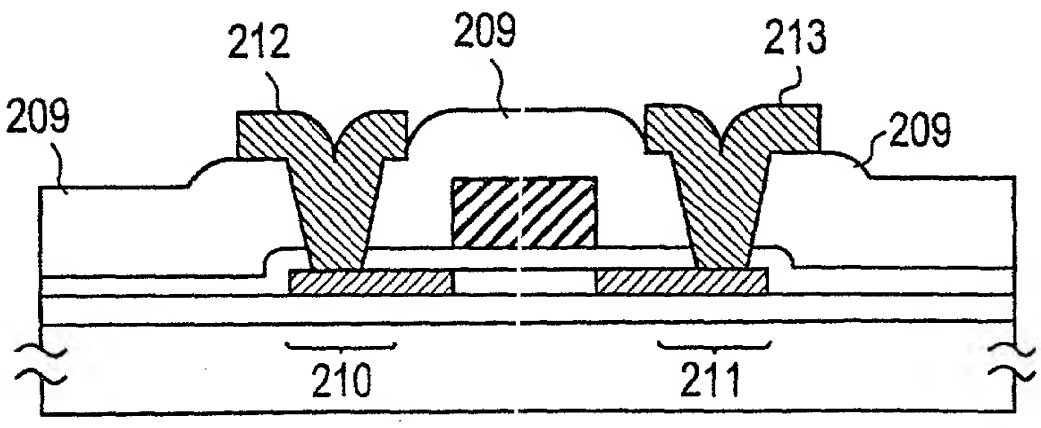


FIG.3

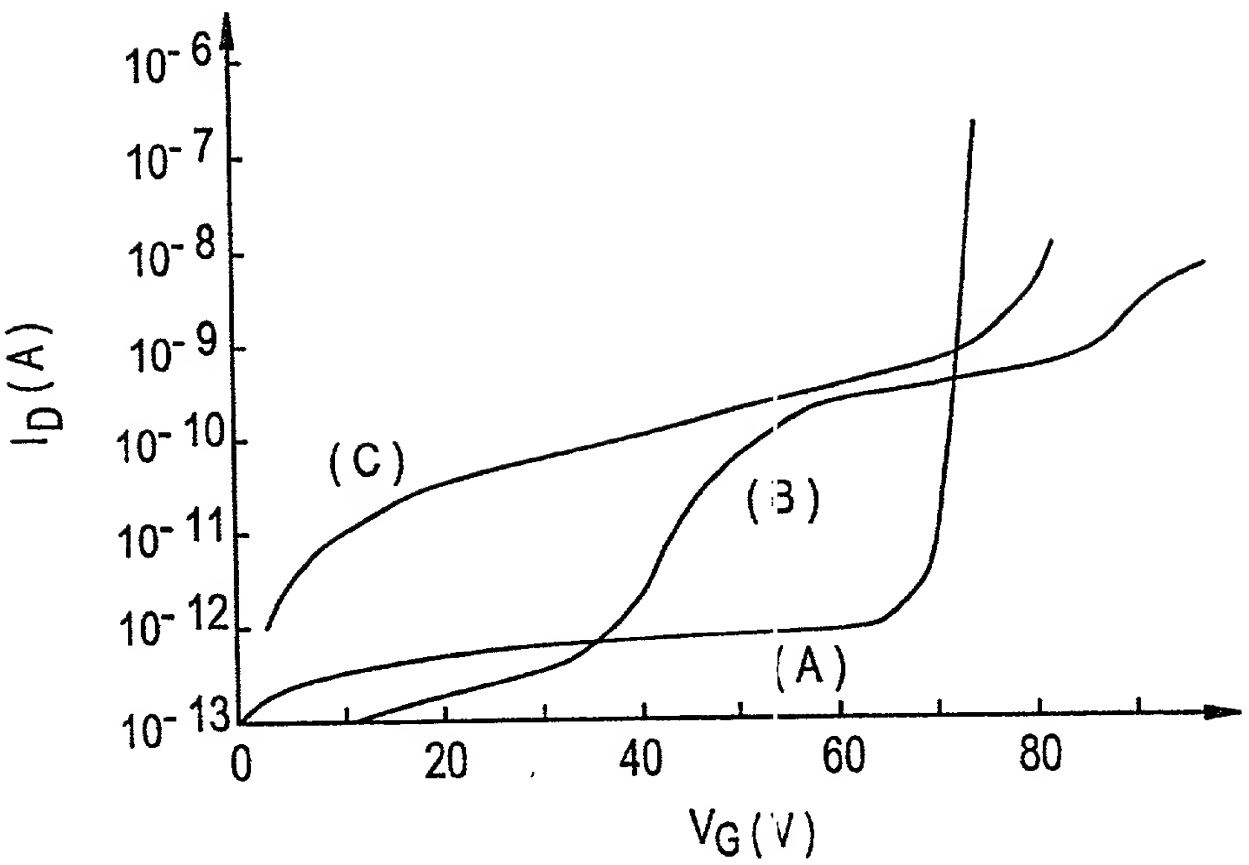


FIG.4A

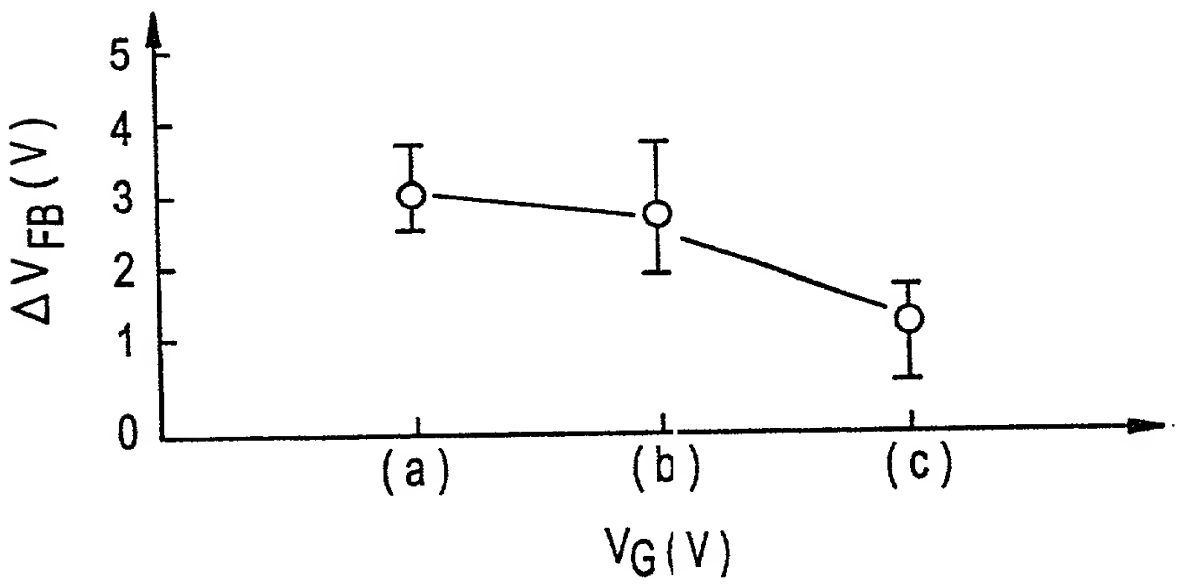
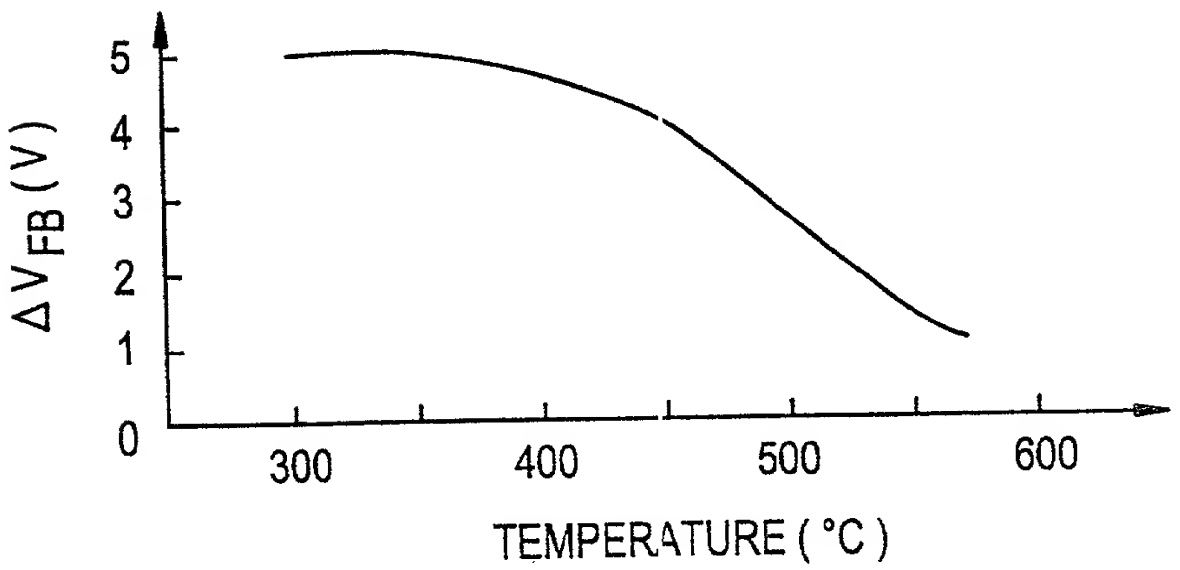


FIG.4B



DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO.
0756-978

PLEASE NOTE: YOU MUST COMPLETE ALL THE FOLLOWING:

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention entitled: * INSULATEING FILM AND METHOD OF PRODUCING SEMICONDUCTOR DEVICE

Insert Title

, the specification of which is attached hereto unless the following box is checked:

Check Box If Appropriate — For Use Without Specification Attached

☒ The specification was filed on Feb. 18, 1994
and was assigned Serial No. 08/198,054
and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows:

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and checked at right:

Insert Priority Information (if appropriate)

Prior Foreign Application(s)			Priority Claimed	
5-55236 (Number)	JAPAN (Country)	Feb. 19, 1993 (Month/Day/Year Filed)	☒ Yes	☐ No
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes	☐ No
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes	☐ No

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months Prior To The Filing Date of This Application:

Country	Application No.	Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status—patented, pending, abandoned)

Revised 11/90

*NOTE: Must be completed.

I hereby appoint the following attorneys to prosecute this application and/or an international application and to transact all business in the Patent and Trademark Office connected therewith:

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PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Insert Name of Non-U.S. firm, attorney or agent

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Insert Full Name of First or Sole Inventor and Date This Document Is Signed	FULL NAME OF SOLE OR FIRST INVENTOR Shunpei YAMAZAKI	INVENTOR'S SIGNATURE Shunpei Yamazaki	DATE 4/8/1994
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Full Name of Seventh Inventor, if any: see above	GIVEN NAME FAMILY NAME	INVENTOR'S SIGNATURE	DATE
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Full Name of Eighth Inventor, if any: see above	GIVEN NAME FAMILY NAME	INVENTOR'S SIGNATURE	DATE
	RESIDENCE (City, State & Country)	CITIZENSHIP	
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Full Name of Ninth Inventor, if any: see above	GIVEN NAME FAMILY NAME	INVENTOR'S SIGNATURE	DATE
	RESIDENCE (City, State & Country)	CITIZENSHIP	
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		
Full Name of Tenth Inventor, if any: see above	GIVEN NAME FAMILY NAME	INVENTOR'S SIGNATURE	DATE
	RESIDENCE (City, State & Country)	CITIZENSHIP	
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Full Name of Eleventh Inventor, if any: see above	GIVEN NAME FAMILY NAME	INVENTOR'S SIGNATURE	DATE
	RESIDENCE (City, State & Country)	CITIZENSHIP	
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		
Full Name of Twelfth Inventor, if any: see above	GIVEN NAME FAMILY NAME	INVENTOR'S SIGNATURE	DATE
	RESIDENCE (City, State & Country)	CITIZENSHIP	
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